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1 [Architecture analysis and automation: Architecture evaluation for power-efficient FPGAs](#)

Fei Li, Deming Chen, Lei He, Jason Cong

 February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(338.83 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents a flexible FPGA architecture evaluation framework, named fpgaEVA-LP, for power efficiency analysis of LUT-based FPGA architectures. Our work has several contributions: (i) We develop a mixed-level FPGA power model that combines switch-level models for interconnects and macromodels for LUTs; (ii) We develop a tool that automatically generates a back-annotated gate-level netlist with post-layout extracted capacitances and delays; (iii) We develop a cycle-accurate power simulator ...

Keywords: FPGA architecture, FPGA power model, low power design

2 [Sequential test generation at the register-transfer and logic levels](#)

Abhijit Ghosh, Srinivas Devadas, A. Richard Newton

 January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(984.27 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The problem of test generation for non-scan sequential VLSI circuits is addressed. A novel method of test generation that efficiently generates test sequences for stuck-at faults in the logic circuit by exploiting register-transfer-level (RTL) design information is presented. Our approach is targeted at chips with data-path like STG. The problem of sequential test generation is decomposed into three subproblems of combinational test generation, fault-free state justification and ...

3 [A parallel embedded-processor architecture for ATM reassembly](#)

Richard F. Hobson, P. S. Wong

 February 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 1

Full text available: pdf(331.21 KB)

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